## REMARKS

Entry of this amendment, reconsideration, and allowance are requested.

Regarding the antecedent basis objection raised with respect to claims 9, 19, and 29. The antecedent basis concerns are remedied by replacing the phrase "said address of said execute block instruction" in claims 9, 19 and 29 by the phrase "an address indicative of a memory location of said execute block instruction." Withdrawal of this objection is appropriate.

All pending claims stand rejected for obvious based on U.S. patent 6,907,598 to Fraser in view of the common general knowledge of the skilled person. In paragraph 27 of the Office Action in the section entitled "Response to Arguments," the Examiner cites a section (pages A42-A44) of the textbook Hennessy et al., *Computer Architecture: A Quantitative Approach*, in support of the knowledge of the skilled person with respect to known techniques for exception handling. This rejection is respectfully traversed.

Fraser lacks two elements recited in independent claim 1. First, The Examiner concedes in paragraph 10 of the Office Action that Fraser does not in fact disclose the following feature of claim 1:

> an exception handling circuit operable upon occurrence of an exception during execution of said block of two or more instructions to store said block count value, and upon completion of handling of said exception, to restart execution of said block of two or more program instructions at a program instruction within said block of two or more instructions indicated by said block count value.

But this is not the only feature of claim 1 not disclosed by Fraser. In particular, Fraser also fails to the follow second feature:

> wherein when executing said block of two or more program instructions, said program counter register is configured to store an

> address indicative of a memory location of said execute block instruction.

At column 12, lines 20-30, Fraser teaches that when the Echo module 336 executes an Echo instruction (which the Examiner contends corresponds to the execute block instruction of claim 1), the PC control module 342 saves the current program counter value to a predetermined location (e.g., a temporary program counter stack), and then "changes the program counter based on a displacement value or parameter indicated by the Echo instruction." (col. 12, lines 23-25; emphasis added).

So Fraser's program counter value is changed during execution of the Echo instruction. Accordingly, Fraser *teaches away from* the subject matter of claim 1 where the address indicative of a memory location of the execute block instruction is stored in the program counter register when executing the block of two or more instructions. While the claimed block counter value changes as the block instructions are executed, the claimed program counter value does not. This difference is a first reason that the rejection should be withdrawn.

Although Fraser does not teach the claimed exception handling circuit, the Examiner contends that known exception handling circuits, as described by Hennessy, could be included to save the processor execution state. The Examiner further contends that because the block count value is part of the execution state, a skilled person would necessarily provide an exception handling circuit that stored the value of this parameter. The Examiner uses an excerpt from Hennessy to support his contentions. But Hennessy teaches on page A43 (at the start of the second paragraph following the three-itemed list):

> After the exception has been handled, special instructions return the processor from the exception by reloading the PCs and restarting the instruction stream.

Accordingly, although the skilled person might have been aware based on the Hennessy text that the program counter value is saved and restored in the event of an exception, it would not have been obvious to that person to store a block count value—in addition to a program counter value—and to restart execution of the block of program instructions corresponding to the instruction within the block that was being executed when the exception occurred. Storage of the block counter value when an exception occurs during execution of the block of two or more instructions, as specified by claim 1 involves an inventive "leap" by the skilled person relative to the disclosure of Fraser in combination with the Hennessy excerpt. Fraser does not explain what to do if an exception occurs during the Echo instruction execution. This deficiency is a second reason the rejection should be withdrawn.

Indeed, as outlined above, since Fraser teaches that the program counter value is modified during execution of the Echo instruction, if the skilled person was to consider modifying the arrangement of Figure 3 of Fraser to include an exception handling circuit, he would consider, in the event of an exception having occurred during the Echo instruction execution and following handling of the exception, that the program counter value should be restored to the previous value by copying in the stored value from the program counter stack (see col. 12, lines 20-22). Neither Fraser nor Hennessy discloses or suggests that the value stored in the program counter register throughout execution of two or more instructions of the block is an address indicative of the memory location of the execute block instruction.

The approach in claim 1 has advantages compared to Fraser. In contrast to Frazer's modifying the program counter value when executing instructions of the Echo instruction (alleged counterpart of execute block instruction), it is easier to integrate the execute block instructions with existing program code for exception handling in the approach of claim 1

because the existing program counter behavior does not need to be significantly changed to compensate for inclusion of the embedded block instructions. Instead, the separate block counter register monitors which of the two or more instructions within the block is currently being executed while the value stored in the program counter register remains static during execution of the plurality of instructions of the embedded block.

The application is in condition for allowance. An early notice to that effect is respectfully submitted. If the Examiner disagrees, Applicant requests that the amendment be entered for purposes of appeal.

Respectfully submitted,

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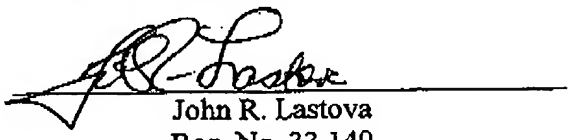
By: 
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